IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) For use in a shared bus system comprising a plurality of bus devices capable of requesting access to a shared bus, a bus arbitrator operable to ~~slowly~~ activate and ~~rapidly~~ de-activate tristate line drivers coupled to said shared bus, said bus arbitrator comprising:

an input circuit capable of receiving a first bus access request signal from a first of said plurality of bus devices and a second bus access request signal from a second of said plurality of bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit capable of receiving said first bus access request signal and generating therefrom a time-delayed first bus access request signal, the delay circuit also capable of receiving said second bus access request signal and generating therefrom a time-delayed second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit capable of ~~receiving said first bus access request signal and said time-delayed first bus access request signal and~~ generating a first line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled, the comparator circuit also capable of generating a second line driver enable signal

only if both of said second bus access request signal and said time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

2. (Currently Amended) The bus arbitrator as set forth in Claim 1 wherein said comparator circuit:

disables said first line driver enable signal if either of said first bus access request signal and said time-delayed first bus access request signal is disabled; and

disables said second line driver enable signal if either of said second bus access request signal and said time-delayed second bus access request signal is disabled.

3. (Currently Amended) The bus arbitrator as set forth in Claim 2 wherein a ~~time~~ the second delay of said delay circuit is greater than a maximum de-activation delay period associated with said tri-state line drivers.

4. (Currently Amended) The bus arbitrator as set forth in Claim 3 wherein said comparator circuit comprises:

a [[n]] first AND gate having a first input for receiving said first bus access request signal and a second input for receiving said time-delayed first bus access request signal; and

a second AND gate having a first input for receiving said second bus access request signal and a second input for receiving said time-delayed second bus access request signal.

5. (Original) The bus arbitrator as set forth in Claim 3 wherein said delay circuit is an asynchronous delay circuit.

6. (Currently Amended) The bus arbitrator as set forth in Claim 5 wherein said delay circuit comprises:

a first set of an even number of inverters connected in series, wherein a first of said ~~even number of~~ inverters in the first set receives said first bus access request signal and a last of said ~~even number of~~ inverters in the first set generates said time-delayed first bus access request signal; and

a second set of an even number of inverters connected in series, wherein a first of said inverters in the second set receives said second bus access request signal and a last of said inverters in the second set generates said time-delayed second bus access request signal.

7. (Original) The bus arbitrator as set forth in Claim 3 wherein said delay circuit is a synchronous delay circuit.

8. (Currently Amended) The bus arbitrator as set forth in Claim 7 wherein said delay circuit comprises:

a first flip-flop having an input capable of receiving said first bus access request signal and an output coupled to said comparator circuit that generates said time-delayed first bus access request signal;

a first inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the first flip-flop;

a second flip-flop having an input capable of receiving said second bus access request signal and an output coupled to said comparator circuit that generates said time-delayed second bus access request signal; and

a second inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the second flip-flop.

9. (Currently Amended) A shared bus system comprising:

N bus devices capable of requesting access to a shared bus;

M tristate line drivers, each of said M tristate line drivers having an input for receiving a logic bit from one of said N bus devices and an output for outputting said received logic bit to said shared bus, wherein said each tristate line driver outputs said received logic bit when a line driver enable signal associated with said each tristate line driver is enabled and an output of said each tristate line driver is put into a high-impedance state when said line driver enable signal is disabled;

a bus arbitrator operable to ~~slowly~~ activate and ~~rapidly~~ de-activate said M tristate line drivers, said bus arbitrator comprising:

an input ~~interface~~ circuit capable of receiving a first bus access request signal from a first of said N bus devices and a second bus access request signal from a second of said N bus devices, the input circuit also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled, the input circuit associated with a first delay;

a delay circuit capable of receiving said first bus access request signal ~~from said input interface~~ and generating therefrom a time-delayed first bus access request signal, the delay circuit also capable of receiving said second bus access request signal and generating therefrom a time-delayed second bus access request signal, the delay circuit associated with a second delay; and

a comparator circuit capable of ~~receiving said first bus access request signal from said input interface and said time-delayed first bus access request signal from said delay circuit and~~ generating a first line driver enable signal only if both of said first bus access request signal and said time-delayed first bus access request signal are enabled, the comparator circuit also capable of generating a second line driver enable signal only if both of said second bus access request signal and said time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but does not delay high-to-low transitions in the first line driver enable signal.

~~a bus keeper capable of holding each line of the shared bus at a particular logic level when all of the tristate line drivers are put into the high impedance state.~~

10. (Currently Amended) The shared bus system as set forth in Claim 9 wherein said comparator circuit:

disables said first line driver enable signal if either of said first bus access request signal and said time-delayed first bus access request signal is disabled; and

disables said second line driver enable signal if either of said second bus access request signal and said time-delayed second bus access request signal is disabled.

11. (Currently Amended) The shared bus system as set forth in Claim 10 wherein ~~a time~~ the second delay of said delay circuit is greater than a maximum de-activation delay period associated with said tri-state line drivers.

12. (Currently Amended) The shared bus system as set forth in Claim 11 wherein said comparator circuit comprises:

a [[n]] first AND gate having a first input for receiving said first bus access request signal and a second input for receiving said time-delayed first bus access request signal; and

a second AND gate having a first input for receiving said second bus access request signal and a second input for receiving said time-delayed second bus access request signal.

13. (Original) The shared bus system as set forth in Claim 11 wherein said delay circuit is an asynchronous delay circuit.

14. (Currently Amended) The shared bus system as set forth in Claim 13 wherein said delay circuit comprises:

a first set of an even number of inverters connected in series, wherein a first of said ~~even number of~~ inverters in the first set receives said first bus access request signal ~~from said input interface~~ and a last of said ~~even number of~~ inverters in the first set generates said time-delayed first bus access request signal; and

a second set of an even number of inverters connected in series, wherein a first of said inverters in the second set receives said second bus access request signal and a last of said inverters in the second set generates said time-delayed second bus access request signal.

15. (Original) The shared bus system as set forth in Claim 11 wherein said delay circuit is a synchronous delay circuit.

16. (Currently Amended) The shared bus system as set forth in Claims 15 wherein said delay circuit comprises:

a first flip-flop having an input capable of receiving said first bus access request signal ~~from said input interface~~ and an output coupled to said comparator circuit that generates said time-delayed first bus access request signal;

a first inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the first flip-flop;

a second flip-flop having an input capable of receiving said second bus access request signal and an output coupled to said comparator circuit that generates said time-delayed second bus access request signal; and

a second inverter having an input capable of receiving the clock signal and an output coupled to a clock input of the second flip-flop.

17. (Currently Amended) For use in a shared bus system comprising N bus devices capable of requesting access to a shared bus, a method for ~~slowly~~ activating and ~~rapidly~~ de-activating a plurality of tristate line drivers coupled between the shared bus and the N bus devices, the method comprising the steps of:

receiving a first bus access request signal from a first of the bus devices;

receiving a second bus access request signal from a second of the bus devices;

blocking the second bus access request signal when the first bus access request signal is enabled, the blocking step associated with a first delay;

generating from the first bus access request signal a time-delayed first bus access request signal and generating from the second bus access request signal a time-delayed second bus access request signal, the generating step associated with a second delay;

comparing ~~in a comparator circuit~~ the first bus access request signal and the time-delayed first bus access request signal and generating a first line driver enable signal only if both of the first bus access request signal and the time-delayed first bus access request signal are enabled; and

comparing the second bus access request signal and the time-delayed second bus access request signal and generating a second line driver enable signal only if both of the second bus access request signal and the time-delayed second bus access request signal are enabled, wherein the second delay delays low-to-high transitions in the line driver enable signals by no more than one-half of a clock cycle of a clock signal, and wherein the first delay delays high-to-low transitions in the second line driver enable signal by an amount less than the second delay but

does not delay high-to-low transitions in the first line driver enable signal.

~~holding each line of the shared bus at a particular logic level when all of the tristate line drivers are put into a high-impedance state.~~

18. (Currently Amended) The method as set forth in Claim 17 further comprising the steps of:

disabling the first line driver enable signal if either of the first bus access request signal and the time-delayed first bus access request signal is disabled; and

disabling the second line driver enable signal if either of the second bus access request signal and the time-delayed second bus access request signal is disabled.

19. (Currently Amended) The method as set forth in Claim 18 wherein ~~a time~~ the second delay ~~associated with the time-delayed first bus access request signal~~ is greater than a maximum de-activation delay period associated with the plurality of tri-state line drivers.

20. (Currently Amended) The method as set forth in Claim 19 wherein the comparing steps comprise using a comparator circuit, the comparator circuit comprising: [[es]]

a [[n]] first AND gate having a first input for receiving the first bus access request signal and a second input for receiving the time-delayed first bus access request signal; and

a second AND gate having a first input for receiving the second bus access request signal and a second input for receiving the time-delayed second bus access request signal.

21. (Previously Presented) The bus arbitrator of Claim 1, wherein the input circuit comprises:

an inverter capable of receiving and inverting the first bus access request signal; and

an AND gate capable of receiving the inverted first bus access request signal and the second bus access request signal, the AND gate also capable of outputting the second bus access request signal when the first bus access request signal is not enabled and blocking the second bus access request signal when the first bus access request signal is enabled.